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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/627,043	07/25/2003	Geoff W. Taylor	OPE-023	3750

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EXAMINER	
VANNUCCI, JAMES	
ART UNIT	**PAPER NUMBER**
2828	

DATE MAILED: 02/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application N .	Applicant(s)	
	10/627,043	TAYLOR ET AL.	
	Examin r	Art Unit	
	Jim Vannucci	2828	

-- The MAILING DATE of this communication appears n the cover sheet with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,7-19,21-31,37-49 and 51-59* is/are rejected.

7)☒ Claim(s) *3-6,20,32-36 and 50* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12-15-03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2, 7-12, 30-31, 37-42 and 59 are rejected under 35 U.S.C. 102(b) as being anticipated by Larkins(5,349,599).

Claims 1, 30 and 59, figure 6 discloses a substrate(2), a multi-layer structure formed on the substrate, an array of thyristor devices(col. 14, lines 56-58) and corresponding resonant cavities(16 & 30) formed in the multi-layer structure where the resonant cavities are adapted to process different wavelengths of light(col. 18, lines 24-27).

Claims 2 and 31, portions of the multi-layer structure are removed to provide the resonant cavities with different vertical dimensions that correspond to the different wavelengths(col. 13, lines 47-49).

Claims 7 and 37, the thyristor device array can be a vertical cavity lasing device(fig. 6) in an array(fig. 18) emitting light at different wavelengths(col. 22, lines 60-66).

Claims 8 and 38, each given thyristor device of the array disclosed in figure 18 is configured as an optical detecting device(col. 22, lines 60-63) to thereby provide an

array of optical detectors that detect input optical pulses at different wavelengths and produces corresponding output pulses.

Claims 9 and 39, the output pulses are electrical output pulses that correspond to detected input optical pulses at different wavelengths(col. 22, lines 60-66).

Claims 10 and 40, figure 22 discloses output pulses that are optical output pulses that correspond to detected input optical pulses at different wavelengths(col. 23, lines 64-66).

Claims 11 and 41, figure 6 discloses a thyristor device with an n-type modulation doped quantum well structure and a p-type modulation doped quantum well structure(16 & 30; and col. 10, lines 64-67).

Claims 12 and 42, a current source coupled to either the n-type modulation doped quantum well structure or the p-type modulation doped quantum well structure is disclosed(col. 16, line 64 to col. 17, line 8).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 13-14, 17, 21-25, 43-44, 47 and 51-55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Larkins in view of Yamazaki et al.(6,127,702).

Larkins does not disclose the recited FET arrangement.

Claims 13 and 43, figure 18A of Yamazaki discloses a p-channel FET transistor formed on a substrate and an n-channel FET transistor formed atop the p-channel FET transistor(col. 22, lines 35-37). If the device disclosed in Larkins is modified to be two stacked FET's, the p-channel FET transistor will be formed from the p-type modulation doped quantum well structure(fig. 6, no. 16) and the n-channel FET transistor will be formed from the n-type modulation doped quantum well structure(fig. 6, no. 30).

Claims 14 and 44, figure 18A of Yamazaki discloses a p-channel FET transistor that includes a bottom active layer(Larkins, no. 16) with a cathode terminal and an n-channel FET transistor that includes a top active layer(Larkins, no. 30) with an anode terminal. The thyristor device disclosed in Larkins has an injector terminal coupled to either the n-type modulation doped quantum well structure or the p-type doped p-type quantum well structure(col. 16, lines 64-66).

Claims 17 and 47, the thyristor device disclosed in figure 6 of Larkins has an ohmic contact layer(37), a metal layer(43) for the anode terminal formed on the ohmic contact layer, and a plurality of p-type layers(22, 24, 18 & 28; and col. 7, lines 58-59) formed between the ohmic contact layer(37) and the n-type modulation doped quantum well structure(16; and col. 10, line 66).

Claims 21 and 51, figure 18 of Larkins discloses a current source(Vs) coupled to an injector terminal that draws bias current from a quantum well structure and a load resistor(R12) coupled to the cathode terminal that biases the thyristor device such that a forward bias exists between the anode and cathode terminals that is less than the maximum forward switching voltage of the thyristor device(fig. 8).

Claims 22 and 52, the thyristor device disclosed in figure 18 of Larkins is configured as an optical detector that detects an incident optical pulse of sufficient intensity at an associated wavelength and produces a corresponding output electrical pulse at the cathode terminal of the given thyristor device.

Claims 23 and 53, the thyristor device disclosed in figure 18 of Larkins is configured such that when an incident optical pulse has sufficient intensity at the associated wavelength a photocurrent is produced in the quantum well channel in excess of the bias current to produce a channel charge that exceeds a critical switching charge causing the thyristor device to switch to the ON state. When the incident optical pulse is terminated, the bias current switches the thyristor device to the OFF state(Larkins, cols. 18-32).

Claims 24 and 54, the thyristor device disclosed in figure 6 of Larkins is configured as a laser emitter that emits an output optical pulse at an associated wavelength in response to an input electrical pulse supplied to the injector terminal.

Claims 25 and 55, the thyristor device disclosed in figure 6 of Larkins is configured such that the input electrical pulse produces current in the quantum well channel in excess of the bias current to produce a channel charge that exceeds a critical switching charge causing the thyristor device to switch to the ON state. When the input electrical pulse is terminated the bias current switches the thyristor device to the OFF state. The current through the thyristor device in the ON state is greater than a characteristic lasing threshold current for the thyristor device(Larkins, col. 18-32).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the FET arrangement disclosed in Yamazaki in the thyristor disclosed in Larkins to suppress short channel effects(abstract) as disclosed in Yamazaki.

5. Claims 26-29 and 56-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Larkins in view of Atanackovic et al.(6,734,453).

Larkins does not disclose a bragg reflector or a diffraction grating.

Claims 26 and 56, figure 9 of Atanackovic discloses resonant cavities that have a bottom distributed Bragg reflector mirror(64). Larkin discloses a top dielectric mirror.

Regarding claims 27 and 57, portions of the multi-layer structure(34) disclosed in Larkins are removed to provide the resonant cavities with different vertical dimensions(col. 13, lines 45-49) and are disposed between the active device structure(30) and the top dielectric mirror.

Claim 28, Larkins discloses means for passing light through the top dielectric mirror and figure 9 of Atanackovic discloses passing light through the bottom distributed Bragg reflector mirror(64) to injected light into the resonant cavity or through which light produced in the resonant cavity is emitted.

Claims 29 and 58, Atanackovic discloses a plurality of diffraction gratings(col. 12, line 58) formed under the top dielectric mirror where the diffraction gratings inject incident light that is propagating along an in-plane direction into the resonant cavities and emits light produced in the resonant cavities along an in-plane direction.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the reflector and grating disclosed in Atanackovic with the device

disclosed in Larkins to direct light in a desired direction as disclosed in Atanackovic(col. 9, lines 43-44).

6. Claims 15-16, 18-19, 45-46 and 48-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Larkins in view of Yamazaki as applied above, and further in view of Wang(6,621,125).

Larkins and Yamazaki do not disclose ion implants.

Claims 15, 18, 45 and 48, figure 2A of Wang discloses an n-type ion implant(36) for improved coupling to a terminal(col. 1, lines 61-65).

Claims 16, 19, 46 and 49, figure 2A of Wang discloses a p-type ion implant(32) for improved coupling to a terminal(col. 1, lines 61-65).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use ion implants as disclosed in Wang with the device disclosed in Larkins and Yamazaki for improved coupling to a terminal as disclosed in Wang.

Allowable Subject Matter

7. Claims 3-6, 20, 32-36 and 50 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter. The following limitations are primarily responsible for distinguishing these claims over the prior art.

Regarding claims 3-6 and 32-36, the limitations concerning the portions of the multi-layer structure that are removed to provide the resonant cavities with different vertical dimensions include a periodic substructure formed by an undoped spacer layer and an undoped etch stop layer that can be repeated.

Regarding claims 20 and 50, the limitations concerning a plurality of p-type layers include a top sheet and bottom sheet of planar doping of highly doped p-material separated by a lightly doped layer of p-material where the top sheet achieves low gate contact resistance and the bottom sheet defines the capacitance of the n-channel FET transistor.

Proper motivation could not be found in the prior art to combine references that disclose these limitations with the references that disclose the other limitations recited in these claims.

Correspondence

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Jim Vannucci whose phone number is (571) 272-1820.

Any inquiry of a general nature or relating to the status of this application should be directed to the Technology Center whose telephone number is (703) 308-0956.

Papers related to Technology Center 2800 applications only may be submitted to Technology Center 2800 by facsimile transmission. Any transmission not to be considered an official response must be clearly marked "DRAFT". The faxing of such

papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Technology Center Fax Center number is (703) 872-9306.

James Vannucci